AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for testing semiconductor devices that output non-deterministic entity information, the method including the steps:

generating test signals with a semiconductor tester;

applying the generated test signals to the device-under-test (DUT);

capturing actual output entities from the DUT in response to the applied generated test signals;

comparing the actual output entities to expected output entities and identifying a fail condition where a comparison fails to match an actual output entity to an expected output entity; and

if a failure is identified in the comparing step, defining a window of valid expected entities and comparing the failed actual output entity to the window of valid expected entities.

2. (Original) A method according to claim 1 and further including the step:

substituting the fail condition with a pass condition where further comparing the failed actual output entity to the window of valid expected entities leads to a match between the failed actual output entity and any one of the valid expected entities in the window.

3. (Currently amended) A method according to claim 1, further comprising ~~wherein the generating test signals includes~~:

generating test program information, including creating a bus layout file.

4. (Original) A method according to claim 3 wherein the creating a bus layout file includes:

identifying the device complexity.

5. (Original) A method according to claim 1, further comprising ~~wherein the step of generating test signals includes~~:

generating test program information, including producing a list of packet and control entities.

6. (Original) A method according to claim 1 wherein each entity comprises a packet or control signal according to a serial or parallel communications protocol.

7. (Original) A method according to claim 4 wherein the step of defining a window includes:

establishing a range of valid entities for the actual entities to fall within based upon the device complexity and typeorder.

8-9. (Canceled).

10. (Currently amended) A computer-readable medium having stored thereon sequences of instructions which, when executed, cause one or more electronic systems to carry out the steps:

generating test signals with a semiconductor tester;

applying the generated test signals to the device-under-test (DUT);

capturing actual output entities from the DUT in response to the applied generated test signals;

comparing the actual output entities to expected output entities and identifying a fail condition where a comparison fails to match an actual output entity to an expected output entity; and

if a failure is identified in the comparing step, defining a window of valid expected entities and comparing the failed actual output entity to the window of valid expected entities.

11. (New) A method for testing a semiconductor device that outputs non-deterministic data, the method comprising:

a) capturing a plurality of actual values output by the semiconductor device, the actual values being in a first sequence, the first sequence comprising a first plurality of ordered sub-parts;

b) indicating whether the plurality of actual values match a plurality of expected values, the expected values being in a second sequence, the second sequence comprising a second plurality of ordered sub-parts; and

c) wherein indicating comprises indicating a match when each of the first plurality of ordered sub-parts matches a matching sub-part of the second plurality of ordered sub-parts, the matching sub-part being offset in the order of the second plurality of

ordered sub-parts by less than a number of sub-parts from a corresponding sub-part, the corresponding sub-part being a subpart of the second plurality of sub-parts corresponding to the sub-part of the first plurality of ordered sub-parts, and the number being greater than one.

12. (New) The method of claim 11, wherein each of the plurality of sub-parts comprises a packet of data.

13. (New) The method of claim 12, wherein capturing a plurality of actual values comprises capturing a plurality of packets output by a communications port on the semiconductor device.

14. (New) The method of claim 11, further comprising indicating that the semiconductor device is manufactured correctly based in part on the indication of whether the plurality of actual values match the plurality of expected values.

15. (New) The method of claim 11, further comprising obtaining the number by performing steps comprising reading a value in a data file associated with the semiconductor device under test.

16. (New) The method of claim 11, wherein indicating whether the plurality of actual values match the plurality of expected values, comprises:

i) comparing each of the first plurality of ordered sub-parts to the corresponding sub-part; and

ii) for each of the first plurality of ordered sub-parts that does not match the corresponding sub-part, comparing the sub-part to one or more sub-parts of the second plurality of ordered sub-parts, the one or more sub-parts being offset by less than the threshold number of sub-parts from the corresponding sub-part.

17. (New) The method of claim 16, wherein comparing the sub-part to one or more sub-parts of the second plurality of ordered sub-parts comprises comparing the subsequence to one or more sub-parts offset from the corresponding sub-part in either a positive or negative direction.